DELAY DEFECTS DIAGNOSIS USING ANNs

Miona Andrejević, Vladimir Petrović, Dejan Mirković, Vančo Litovski
Faculty of Electronic Engineering Niš

Abstract - *In this paper artificial neural networks (ANNs) are applied to diagnosis of delay defects in the digital part of a nonlinear mixed-mode circuit. The approach is demonstrated on the example of a relatively complex sigma-delta modulator. Defects in this example are delays of rising and falling edge of digital signals. Fault dictionary is created, by simulation, using the response of the circuit to an input ramp signal. It is represented in a form of a look-up table. Artificial neural network is then trained for modeling (memorizing) the look-up table. The diagnosis is performed so that the ANN is excited by faulty responses in order to present the fault codes at its output. There were no errors in identifying the faults during diagnosis.*

1. INTRODUCTION

Every complex system is liable to faults or failures. In most general terms a fault is any change in a system that prevents it from operating in the proper manner. We define diagnosis as the task of identifying the cause of a fault that is manifested by some observed behavior. Then some method of determining what fault has occurred is required. This is most often considered to be a two-stage process: firstly the fact that fault has occurred must be recognized – what is referred to as fault detection. Secondly, the nature should be determined such that appropriate remedial action may be initiated.

The explosion of integrated circuit technology has brought with it some difficult testing problems. The recent growth of mixed analogue and digital circuits complicates the testing problem even further. It becomes more complicated to determine a set of input test signals and output measurements that will provide a high degree of fault coverage. There is also a timing problem of testing the circuits even on the fastest automated equipment.

In this paper we will show that feed-forward ANN may be applied to the diagnosis of non-linear dynamic electronic circuits that are mixed with digital ones. A specific example is chosen, i.e. effects of rising and falling edge delays in digital circuits are considered.

The simulation before test concept was adopted. This means that after choosing the set of faults of interest (say the most probable ones), repetitive simulation is performed in order to create the system response for every fault. Codes are associated to the responses and used as part of the fault dictionary that, in addition, contains the faulty responses themselves. Of cause, the responses are represented in a form that is easy to manipulate.

The ANN is first trained for modeling the look-up table. This means that faulty responses are repeatedly brought to the input, while the ANN is forced to present the fault codes at its output. Then, the ANN running with the given vector of stimuli (measured output signals of a faulty or, possibly, fault free system) may be viewed as search of the look-up table. The ANN response, if the network properly trained, will immediately find the fault and produce the fault code at its output.

The procedure applied is reminiscent to the one implemented to analog circuits in [1]. To our knowledge this is the first application of ANNs to diagnosis of mixed signal circuit.

2. CONCEPTS OF DIAGNOSIS

Besides the human expert that is usually performing the diagnostic project, one needs tools that will help, and what is most desired, will perform diagnosis automatically. Such tools are a great challenge to design engineers that pertains to the fact that generally the diagnostic problem is indeterminate. In addition, it is a deductive process with one set of data creating, in general, unlimited number of hypotheses among which one should try to find the solution. This is why permanent attention of the research community is attracted by this problem [2].

During the life-cycle of a product, testing is implemented in both the production phase and the implementation phase. We claim, however, that the sustainability of a product is strongly influenced by the design phase. So, to make a sustainable product, one should design the test procedure and synthesize test signals early in the design phase.

It is frequently possible to perform functional verification of the system. That, most frequently, happens when a small number of input/output terminals is present. In the majority of cases however, full functional testing becomes time consuming and is not acceptable. So, one applies defect-oriented (structural) testing, as will be discussed in more detail as follows.

We consider testing to be: the selection of a set of defects regarded as the most probable, the description of a set of measurements, the selection of a set testing points (or output signals) and most importantly, the synthesis of optimal testing signals that will be applied at the system inputs allowing for detectability and observability of the listed fault effects. Here, optimality means that one test signal covers as many faults as possible.

Selection of the type of measurements and testing points is specific to the circuit. One should stick to those measurements that are prescribed for functional verification. Specific measurements such as supply current monitoring are frequently adopted, too. Separate test points may be added in order to improve detectability or observability. Specific design for testability concepts can be applied.

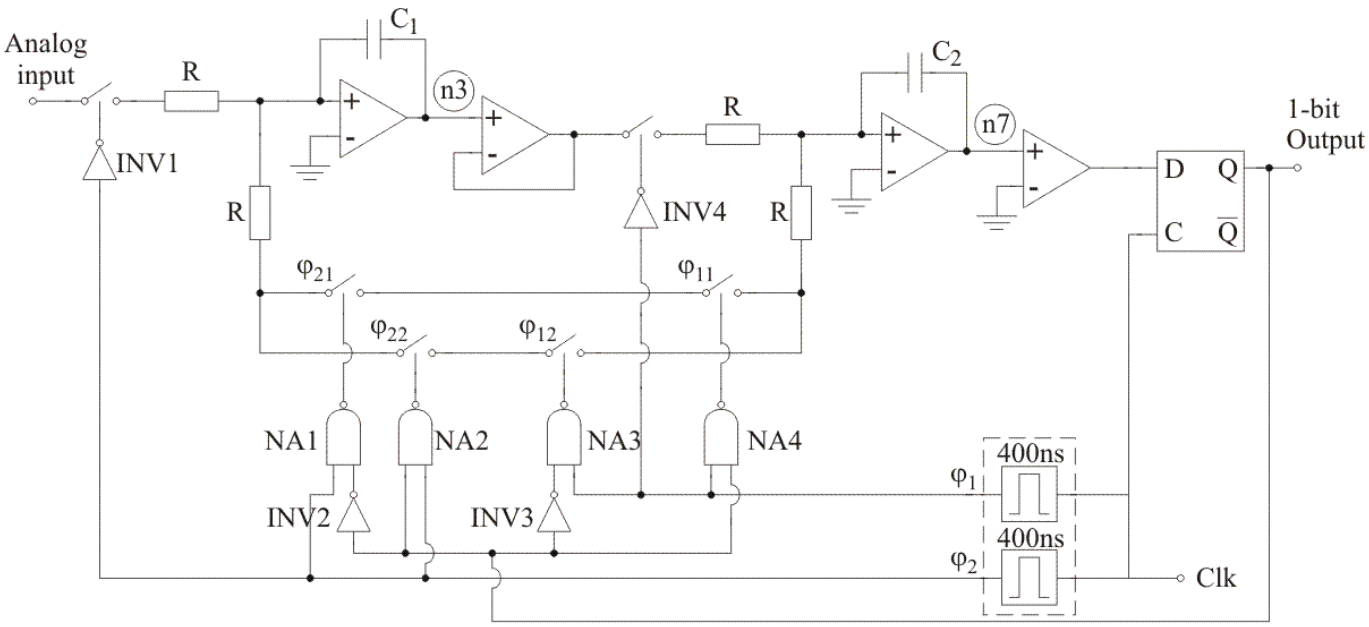

Fig. 1. *Sigma-delta modulator architecture*

After selection of test signals, the fault coverage has to be evaluated. To do that, as many replicas of the original circuit as the number of predicted faults have to be created. For large complex systems containing mechanical, analogue and digital parts, the number of replicas becomes huge. Each replica has one fault inserted. The fault coverage is evaluated after simulation of the faulty systems by comparing the results thus obtained with the response of the fault-free system. If these two differ, the fault is covered and the corresponding entry in the fault list can be removed. To reduce the computational effort, algorithms have been proposed to simulate multiple faulty circuits concurrently in both the analogue and the digital domains but not in mixed signal, and mixed description systems.

3. SIGMA-DELTA MODULATOR ARCHITECTURE

Sigma-delta modulators are very attractive for design low frequency high-resolution analog-to-digital converters. Sigma-delta modulators trade speed for resolution. They employ coarse quantization in one or more feedback loops. By sampling at a frequency that is much greater than the signal bandwidth, it is possible for the feedback loops to shape the quantization noise so that most of the noise power is shifted out of the signal band. The out of band noise can then be attenuated with a digital filter. The degree to which the quantization noise can be attenuated depends on the order of the noise shaping and the oversampling ratio [3].

In addition to their tolerance for circuit nonidealities, oversampled A/D converters simplify system integration by reducing the burden on the supporting analog circuitry. Because they sample the analog input signal at well above the Nyquist rate, precision sample-and-hold circuitry is unnecessary. Also, the burden of analog antialiasing filter is considerably reduced. Much of its function is transferred to the digital decimation filter, which can be designed and manufactured to precise specifications, including a linear phase characteristic.

4. FAULTS DIAGNOSIS IN THE EXAMPLE CIRCUIT

As an example of a complex circuit, the sigma-delta modulator in Fig. 1 is chosen [2].

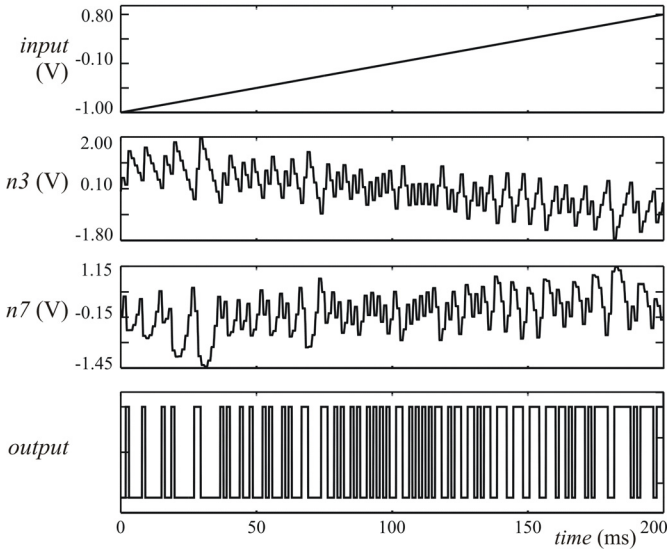

Fig. 2. *Simulation results for ramp excitation*

This is a mixed-signal circuit, having both analogue and digital elements. Switches in the circuit are modeled as truly ideal switches, with zero resistance for closed switch and infinite resistance for open switch. Simulations are performed using Alecsis [4] simulator.

The integrator charging time is invariable with respect to clock rate in order to keep the gain constant. This means that

the analog switch must be turned on for fixed time duration regardless of clock rate. This is achieved by using monostable multivibrator as a fixed-width pulse generator in the circuit.

Table 1. Fault dictionary

Defect code	Defect type	Signature
0	FF	20440480A
1	inv3(tf=50ns)	402804411
2	na1(tr=250ns)	149463131
3	na1(tr=400ns)	31C352C66
4	na1(tf=50ns)	100110012
5	na1(tf=100ns)	008000010
6	na2(tf=50ns)	404811044
7	na3(tr=400ns)	102104208
8	na2(tf=150ns)	811104844
9	na3(tf=150ns)	030018090
10	na4(tr=100ns)	204110210
11	na1(tf=150ns)	000000000
12	inv1(tf=100ns)	848504890
13	na2(tr=100ns)	102081042
14	na2(tf=100ns)	410842209
15	inv3(tr=100ns)	202404410
16	na3(tr=100ns)	808809021
17	inv1(tr=100ns)	004020040
18	na2(tr=400ns)	020101008
19	inv4(tr=50ns)	088108210
20	inv1(tf=50ns)	811105024
21	na4(tf=50ns)	402804420
22	inv3(tr=50ns)	204208410
23	inv4(tf=100ns)	220220821
24	na4(tf=150ns)	802408811
25	inv3(tr=150ns)	104208210
26	inv4(tr=100ns)	050050110
27	na3(tr=250ns)	021041084
28	inv4(tr=150ns)	0440900C0
29	na1(tr=100ns)	844889112
30	na3(tf=100ns)	082202208
31	inv4(tf=50ns)	208210420
32	na4(tf=100ns)	404210240
33	inv3(tr=150ns)	104208210
34	inv1(tf=150ns)	092430918
35	na3(tf=50ns)	104108210
36	inv1(tr=50ns)	040810108
37	inv3(tf=150ns)	802408420
38	inv4(tf=150ns)	010840882
39	na2(tr=250ns)	080408104
40	inv1(tr=150ns)	000010010

The monostable multivibrator between the clock input and switch control block functions as a pulse generator to produce control signals of fixed time duration. Fig. 2 shows reaction of the system when the input is excited by a ramp signal.

We consider here delays of rising and falling edge of output digital signals as defects to be diagnosed. These defects are neither catastrophic, nor parametric, because there is no change in circuit topology, and no change in element values.

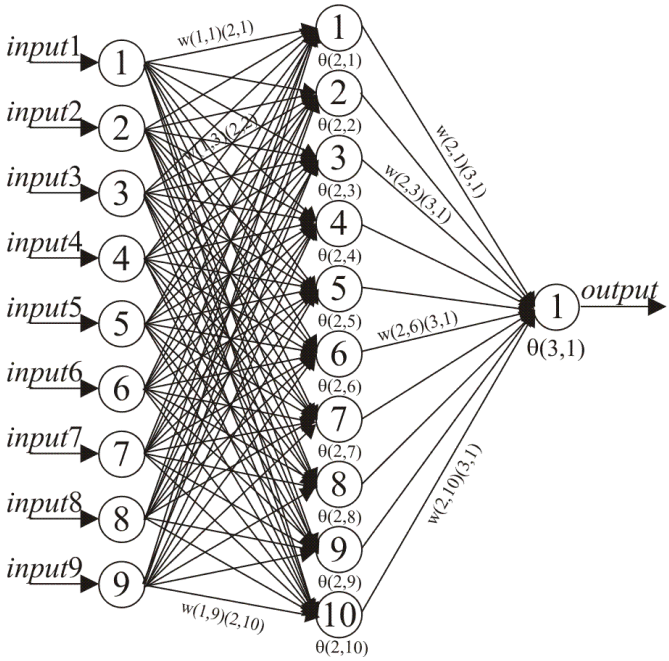

Fig. 3. The diagnostic ANN

Having in mind that clock period in the circuit is 1.2μs (half period is 600ns), we examined effects of delays not greater than 400ns. In fact, effects of rising edge delay are simulated for values of delay: 100ns, 250ns, 400ns, and for falling edge, we simulated smaller values: 50ns, 100ns, 150ns. The goal was to determine how these delays influence the output, and whether different delay values produce different outputs. All digital gates are examined (4 inverters and 4 nand circuits). The first conclusion was that delays in the INV2 circuit do not influence output signal, meaning that output is not changed. Further, there exist group of delays causing the same effect, but it is out of the scope of this paper.

Fault dictionary is created using the response of the circuit to an input ramp signal. The circuit output value is registered after every clock period, so these output digital values form the output signature. These are then represented in more compact hexadecimal presentation. Accordingly, fault dictionary is created as shown in Table 1. It must be noted that defects are coded randomly, while it is very important that defects with similar signatures must not have similar fault codes (for example response 99999 and AAAAA (hexadecimal value *A* is presented to the neural network as decimal value *10*)). If this happens, it may be very difficult, or even impossible for ANN to recognize defects. In

the first column of Table 1, defects are coded. Second column describes the type of the defect, relative to notation given in Fig. 1 (*inv3*(*tf*=50ns) stands for falling edge delay in inverter 3). FF stands for the fault free circuit, and *tr* is for rising edge. The third column contains the signature seen at the output.

Artificial neural network was trained for modeling the look-up table. It is a feed-forward neural network with one hidden layer. The structure of the network is shown in Figure 3. The signatures are inputs to the network, and the fault code is network output to be learned. It means that the neural network has nine inputs (one input per hexadecimal digit) and one output neuron. Hexadecimal values are presented as decimal when they are inputs to the network. After learning was completed, the number of hidden neurons in the resulting ANN was ten, what was found by trial and error after several iterations starting with an estimation based on [5], and [6].

Table 2. ANN output results

Defect code	Signatures presented to ANN inputs	ANN output
0	2 0 4 4 0 4 8 0 10	-0.0002128
1	4 0 2 8 0 4 4 1 1	0.999733
3	3 1 12 3 5 2 12 6 6	2.99978
4	1 0 0 1 1 0 0 1 2	3.99978
5	0 0 8 0 0 0 0 1 0	4.99995
7	1 0 2 1 0 4 2 0 8	6.99983
8	8 1 1 1 0 4 8 4 4	7.99969
9	0 3 0 0 1 8 0 9 0	8.99981
11	0 0 0 0 0 0 0 0 0	10.9999
12	8 4 8 5 0 4 8 9 0	11.9999
13	1 0 2 0 8 1 0 4 2	12.9999
15	2 0 2 4 0 4 4 1 0	14.9998
16	8 0 8 8 0 9 0 2 1	15.9999
17	0 0 4 0 2 0 0 4 0	16.9999
18	0 2 0 1 0 1 0 0 8	17.9998
20	8 1 1 1 0 5 0 2 4	19.9999
21	4 0 2 8 0 4 4 2 0	20.9999
22	2 0 4 2 0 8 4 1 0	21.9999
24	8 0 2 4 0 8 8 1 1	23.9999
25	1 0 4 2 0 8 2 1 0	24.9999
26	0 5 0 0 5 0 1 1 0	25.9998
28	0 4 4 0 9 0 0 12 0	27.9998
29	8 4 4 8 8 9 1 1 2	28.9999
31	2 0 8 2 1 0 4 2 0	30.9998
32	4 0 4 2 1 0 2 4 0	31.9998
34	0 9 2 4 3 0 9 1 8	34
35	1 0 4 1 0 8 2 1 0	34.9999
37	8 0 2 4 0 8 4 2 0	36.9999
38	0 1 0 8 4 0 8 8 2	37.9996
39	0 8 0 4 0 8 1 0 4	39.0009

The structure of the obtained ANN is verified by exciting the ANN with faulty inputs. Responses of the ANN show that there were no errors in identifying the faults what is presented in Table 2. Not all the responses are given in the table, for practical reasons. Note that hexadecimal values are presented as decimal in the table, because decimals are ANN inputs.

7. CONCLUSION

Delay effects in sigma-delta modulator were examined. The diagnosis was successful. Accordingly, we may conclude that ANNs are convenient and powerful means for diagnosis, and, what is important, realizable as a hardware that may be as fast as necessary to follow the changes of the system's response in real time.

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Sadržaj – U ovom radu su veštačke neuronske mreže primenjene na dijagnostiku defekata kašnjenja u digitalnom delu nelinearnog hibridnog kola. Pristup je pokazan na primeru relativno složenog kola sigma-delta modulatora. Defekti koji se posmatraju su kašnjenja rastuće i opadajuće ivice digitalnog signala. Rečnik defekata se formira na osnovu rezultata simulacije, korišćenjem odziva kola na ulazni linearno rastući signal. Rečnik je predstavljen kao tabela pretraživanja. Zatim se obučava veštačka neuronska mreža za modelovanje tabele pretraživanja. Dijagnostika se obavlja tako što se veštačka neuronska mreža pobuđuje odzivima kola sa defektom (kašnjenjem), sa ciljem da se na njenom izlazu generiše kod defekta. Nije bilo grešaka u postupku dijagnostike defekata.

DIJAGNOSTIKA DEFEKATA KAŠNJENJA KORIŠĆENJEM VEŠTAČKIH NEURONSKIH MREŽA

Miona Andrejević, Vladimir Petrović,
Dejan Mirković, Vančo Litovski